

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The invention is described by way of example with reference to the accompanying drawings, wherein:

[0005] Figure 1 is a perspective view illustrating one multi-layer construction of a polymer memory in exploded form;

[0006] Figure 2 is a block diagram illustrating various substructures of the polymer memory, including underlying electronics, the multi-layered construction of Figure 1, and alternating insulating layers and further multi-layered constructions;

[0007] Figure 3 is a top plan view illustrating an array of polymer memory cells that are defined by word and bit lines;

[0008] Figures 4A-⁴~~D~~ represent how each one of the polymer memory cells is written to or read from; and

[0009] Figure 5 is a block diagram of a computer system that may include the polymer memory of Figure 2.